SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech. II Year I Semester Regular & Supplementary Examinations November-2025
DIGITAL LOGIC AND COMPUTER ORGANIZATION
(Common to CSIT, CSE, CIC, CCC & CIA)

Time: 3 Hours   **Max. Marks: 70**

PART-A
(Answer all the Questions 10 x 2 = 20 Marks)

1	a	List out the names of basic logical operators.	CO1	L1	2M
	b	List the names of universal gates with symbols.	CO1	L1	2M
	c	List the types of Buses.	CO2	L1	2M
	d	List the Classification of Computer Generations.	CO2	L1	2M
	e	Represent -7 in signed magnitude, 1s complement and 2s complement.	CO3	L1	2M
	f	What is the advantage of using Booth algorithm?	CO3	L1	2M
	g	Define virtual memory.	CO4	L1	2M
	h	Define main memory and auxiliary memory.	CO4	L1	2M
	i	Classify interface circuits.	CO5	L2	2M
	j	What are the examples of processor?	CO5	L1	2M

PART-B
(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	a	Convert the following into decimal into hexa decimal i) $(5386.34)_{10}$ ii) $(214.35)_{10}$	CO1	L2	5M
	b	Simplify the given Boolean expression using K-map $F(A,B,C,D)= \sum m(0,2,3,8,10,11,12,14)$	CO1	L4	5M

OR

3	a	Define Decoder and explain in detail about a 2-to-4-line binary decoder.	CO1	L1	5M
	b	Design and draw a full adder circuit.	CO1	L6	5M

UNIT-II

4		Define a Register. Explain in detail about various Shift Registers.	CO2	L1	10M

OR

5	a	Explain briefly about the multiprocessors and multi computers of a computer.	CO2	L2	5M
	b	List the different types of a computer.	CO2	L1	5M

UNIT-III

6		Explain the fundamental concept in processor organization.	CO3	L3	10M

OR

7	a	Illustrate the steps in Booth multiplication flow chart. Show the step by step signed multiplication of (-7) and (-11) using Booth algorithm.	CO3	L3	5M
	b	Differentiate between Hardwired Control and Micro-programmed control.	CO3	L2	5M

UNIT-IV

8	a	Describe about memory hierarchy concept in detail.	CO4	L2	5M
	b	Distinguish between SRAM & DRAM.	CO4	L2	5M

OR

9	a	Describe in detail about the memory management requirements.	CO4	L1	5M
	b	Compare Cache and Auxiliary memories.	CO4	L2	5M

UNIT-V

10		Explain the standard I/O devices.	CO5	L2	10M

OR

11	a	Explain the interrupt Nesting.	CO5	L3	5M
	b	Explain about SCSI BUS in detail.	CO5	L2	5M

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